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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,926	11/13/2003	Phillip J. Restle	YOR920030364US1	9879

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,926	RESTLE, PHILLIP J.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-31* is/are allowed.

6)☒ Claim(s) *1,16,17 and 25* is/are rejected.

7)☒ Claim(s) *2-15,18-24 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of "plurality of functional units distributed on said chip" of claim 17, plurality of noise compensation circuits, each gating a global clock to a respective one of said units" of claim 25 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Duley (USP 5,561,389). Figure 5 shows a supply noise compensation circuit sensing the onset of noise events on a supply (44) and selectively gating off/forcing on a chip clock (CLK) to chip circuits (CPU) as called for in claim 1.

Regarding claim 16, the dI/dt is noise associated with the inductance inherently present in the power supply source.

Regarding claim 17, the CPU comprises plurality of functional units, each of the functional units operating with a common power supply VDD, a noise compensation circuit (42) sensing the onset of noise events on a supply (44) and selectively gating off/forcing on a chip clock (CLK) to chip circuits (CPU).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeon (USP 6,621,311). Figure 2 shows a supply noise compensation circuit sensing the onset of noise events on a supply (22) and selectively gating off/forcing on a chip clock (CLK) to chip circuits (internal circuits not shown) as called for in claim 1.

Regarding claim 16, the dI/dt is noise associated with the inductance inherently present in the power supply source.

Regarding claim 17, the internal circuits comprises plurality of functional units, each of the functional units operating with a common power supply VDD, a noise compensation circuit (22) sensing the onset of noise events on a supply and selectively gating off/forcing on a chip clock (CLK) to chip circuits (internal circuits).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duley (USP 5,561,309). Figure 5 of Duley an IC comprising a CPU having a plurality of functional units, each of the functional units operating with a common power supply VDD, a noise compensation circuit (42) sensing the onset of noise events on a supply (44) and selectively gating off/forcing on a chip clock (CLK) to chip circuits (CPU). What not shown in Duley is a plurality of noise compensation circuit for each respective functional units as called for in claim 25. However, one skilled in the art would have recognize that providing each respective functional unit with a corresponding noise compensation circuit is an obvious variation arrangement of Duley's circuit. Such a variation would deem to ensure the proper operation of each functional unit. Therefore,

outside of non-obvious results, the obviousness of using a plurality of noise compensation circuit will not be patentable under 35USC 103(a).

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeon (USP 6,621,311). Figure 2 of Jeon an IC comprising internal circuits having a plurality of functional units, each of the functional units operating with a common power supply POWER, a noise compensation circuit (22) sensing the onset of noise events on a supply (POWER) and selectively gating off/forcing on a chip clock (CLK) to chip circuits (internal circuits). What not shown in Jeon is a plurality of noise compensation circuit for each respective functional units as called for in claim 25. However, one skilled in the art would have recognize that providing each respective functional unit with a corresponding noise compensation circuit is an obvious variation arrangement of Jeon's circuit. Such a variation would deem to ensure the proper operation of each functional unit. Therefore, outside of non-obvious results, the obviousness of using a plurality of noise compensation circuit will not be patentable under 35USC 103(a).

Allowable Subject Matter

7. Claims 2-15, 18-24 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 27-31 are presently allowed.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

10/13/2004